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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/528,714	SUNAYAMA ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *22 February 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 have been considered. Claims 1 and 9-17 have been amended as per Applicant's request.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5, 6, 8, 9, 10, 12, 13, 14, 15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa, U.S. Patent Number 5,142,630 (herein referred to as Ishikawa) in view of Grochowski et al., U.S. Patent Number 5,442,756 (herein referred to as Grochowski) and in further view of Tran, U.S. Patent Number 5,752,259 (herein referred to as Tran).

4. Referring to claim 1, Ishikawa has taught an instruction processing device provided with an instruction fetch pipeline and an instruction execution pipeline and performing an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

a. A storage circuit storing a combination of address mode information of a fetched instruction and an instruction address of the fetched instruction (Ishikawa column 1, lines 43-52).

b. A branch instruction control circuit controlling a branch instruction using the address mode information if the fetched instruction is the branch instruction stored in the storage circuit (Ishikawa column 2, lines 29-50).

c. A transfer circuit transferring the address mode information stored in the storage circuit to the branch instruction control circuit when the branch instruction is executed (Ishikawa column 4, lines 20-27 and Figure 1, element 11).

d. The branch instruction control circuit controlling the branch instruction using the address mode information transferred thereto, as a branch destination of the branch instruction if the branch instruction is not accompanied by an address mode change (Ishikawa column 4, lines 20-27; Figure 2; and Figure 11).

5. Ishikawa has not explicitly taught a pipeline

a. A storage circuit storing after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the instruction execution pipeline.

b. A branch instruction control circuit controlling after the fetched instruction is decoded in the decoding cycle.

c. A transfer circuit transferring in an execution cycle of the instruction execution pipeline.

6. However, Ishikawa has taught that there are cycles performing operations before the execution cycle of instructions (Ishikawa column 2, lines 40-51 and column 4, lines 52-59). Grochowski has taught pipelining processor with

a. A storage circuit storing after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a

decoding cycle of the instruction execution pipeline (Grochowski column 7, lines 7-10; 27-32; and 42-60 and Figure 1).

b. A branch instruction control circuit controlling after the fetched instruction is decoded in the decoding cycle (Grochowski column 7, lines 7-10 and 30-34; column 7, line 61 to column 8, line 12; and Figure 1).

c. A transfer circuit transferring in an execution cycle of the instruction execution pipeline (Grochowski column 7, lines 7-10 and 34-41; column 8, lines 13-31; and Figure 1).

7. A person of ordinary skill in the art at the time the invention was made, and as supported by Grochowski, would have recognized that a pipeline divides the multiple cycles it takes to execute an instruction into steps or stages to overlap execution of instructions, which increases instruction processing speed (Grochowski column 1, lines 46-47 and column 2, lines 10-48). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipeline of Grochowski in the device of Ishikawa to increase processing speed.

8. In addition, Ishikawa has not taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system. Tran has taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system (Tran Abstract, lines 2-17; column 3, lines 22-51; column 5, lines 23-62; and column 8, lines 17-22). In regards to Tran, fetching instructions concurrently is out-of-order, meaning the instructions are not sequentially fetched. A person of ordinary skill in the art at the time the invention was made, and as supported by Tran, would have recognized that, by fetching and executing the instructions out of order, the pipeline is

fully utilized (Tran column 3, lines 42-44), thereby increasing performance (Tran column 3, lines 44-45). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the out-of-order system of Tran in the device of Ishikawa to increase processor performance.

9. Referring to claim 2, Ishikawa has taught wherein said branch instruction control circuit stores a combination of the address mode information of the branch destination of the branch instruction and an instruction address of the branch destination (Ishikawa column 1, lines 43-52).

10. Referring to claim 3, Ishikawa has taught wherein said branch instruction control circuit generates the address mode information of the branch destination based on the address mode information of the branch instruction (Ishikawa column 4, lines 44-59).

11. Referring to claim 5, Ishikawa has taught wherein said branch instruction control circuit outputs a signal indicating the address mode information and instruction address of the branch destination when issuing a branch destination instruction fetch request (Ishikawa column 4, lines 44-59). Ishikawa has not explicitly taught the instruction fetch pipeline. However, Ishikawa has taught that there are cycles performing operations before the execution cycle of instructions (Ishikawa column 2, lines 40-51 and column 4, lines 52-59). Grochowski has taught the instruction fetch pipeline (Grochowski column 7, lines 7-10 and Figure 1). A person of ordinary skill in the art at the time the invention was made, and as supported by Grochowski, would have recognized that a pipeline divides the multiple cycles it takes to execute an instruction into steps or stages to overlap execution of instructions, which increases instruction processing speed (Grochowski column 1, lines 46-47 and column 2, lines 10-48). Therefore, it would have been obvious

to a person of ordinary skill in the art at the time the invention was made to incorporate the pipeline of Grochowski in the device of Ishikawa to increase processing speed.

12. Referring to claim 6, Ishikawa has taught wherein said branch instruction control circuit outputs a signal indicating whether the branch instruction is accompanied by the address mode change when control of the branch instruction is terminated (Ishikawa column 4, lines 33-44). In regards to Ishikawa, it is inherent that there is a signal indicating an address mode change in order to load the address mode bit register.

13. Referring to claim 8, Ishikawa has taught the device further comprising:

a. A branch destination address generation circuit generating an instruction address of the branch destination of the branch instruction using the address mode information stored in the storage circuit (Ishikawa column 2, lines 29-50).

b. Wherein said transfer circuit transfers the address mode information stored in the storage circuit to the branch destination address generation circuit when the branch instruction is executed (Ishikawa column 4, lines 20-27).

14. Referring to claim 9, Ishikawa has taught an instruction processing device provided with an instruction fetch pipeline and an instruction execution pipeline and performing an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

a. A storage circuit storing a combination of mode information of a fetched instruction and an instruction address of the fetched instruction (Ishikawa column 1, lines 43-52).

b. A branch instruction control circuit controlling a branch instruction using the mode information stored in the storage circuit if the fetched instruction is the branch instruction (Ishikawa column 2, lines 29-50).

c. A transfer circuit transferring the mode information stored in the storage circuit to the branch instruction control circuit when the branch instruction is executed (Ishikawa column 4, lines 20-27).

d. The branch instruction control circuit controlling the branch instruction using the mode information transferred thereto as a branch destination of the branch instruction if the branch instruction is not accompanied by a mode change (Ishikawa column 4, lines 20-27; Figure 2; and Figure 11).

15. Ishikawa has not explicitly taught a pipeline

a. A storage circuit storing after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the instruction execution pipeline;

b. A branch instruction control circuit controlling after the fetched instruction is decoded in the decoding cycle; and

c. A transfer circuit transferring in an execution cycle of the instruction execution pipeline.

16. However, Ishikawa has taught that there are cycles performing operations before the execution cycle of instructions (Ishikawa column 2, lines 40-51 and column 4, lines 52-59). Grochowski has taught pipelining processor with

a. A storage circuit storing after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a

decoding cycle of the instruction execution pipeline (Grochowski column 7, lines 7-10; 27-32; and 42-60 and Figure 1);

b. A branch instruction control circuit controlling after the fetched instruction is decoded in the decoding cycle (Grochowski column 7, lines 7-10 and 30-34; column 7, line 61 to column 8, line 12; and Figure 1); and

c. A transfer circuit transferring in an execution cycle of the instruction execution pipeline (Grochowski column 7, lines 7-10 and 34-41; column 8, lines 13-31; and Figure 1).

17. A person of ordinary skill in the art at the time the invention was made, and as supported by Grochowski, would have recognized that a pipeline divides the multiple cycles it takes to execute an instruction into steps or stages to overlap execution of instructions, which increases instruction processing speed (Grochowski column 1, lines 46-47 and column 2, lines 10-48). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipeline of Grochowski in the device of Ishikawa to increase processing speed.

18. In addition, Ishikawa has not taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system. Tran has taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system (Tran Abstract, lines 2-17; column 3, lines 22-51; column 5, lines 23-62; and column 8, lines 17-22). In regards to Tran, fetching instructions concurrently is out-of-order, meaning the instructions are not sequentially fetched. A person of ordinary skill in the art at the time the invention was made, and as supported by Tran, would have recognized that, by fetching and executing the instructions out of order, the pipeline is

fully utilized (Tran column 3, lines 42-44), thereby increasing performance (Tran column 3, lines 44-45). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the out-of-order system of Tran in the device of Ishikawa to increase processor performance.

19. Referring to claim 10, Ishikawa has taught an instruction processing device provided with an instruction fetch pipeline and an instruction execution pipeline and performing an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

a. A fetch circuit fetching an instruction (Ishikawa column 3, lines 23-25). In regards to Ishikawa, in order to fetch an instruction there must be a fetch circuit.

b. A storage circuit storing mode information of each fetched instruction as part of an instruction address of the fetched instruction that has been stored (Ishikawa column 1, lines 43-52).

c. A control circuit controlling an instruction process of each instruction based on the stored mode information (Ishikawa column 3, lines 25-35 and 43-65).

d. The control circuit controlling a branch instruction using the mode information that has been stored as mode information of a branch destination of the branch instruction if the fetched instruction is the branch instruction and is not accompanied by a mode change (Ishikawa column 4, lines 20-27; Figure 2; and Figure 11).

20. Ishikawa has not explicitly taught a pipeline

a. An instruction fetch pipeline;

b. A storage circuit storing after an instruction fetch request is issued and before each fetch instruction is decoded in a decoding cycle of the instruction execution pipeline; and

c. A control circuit controlling after the fetched instruction is decoded hi the decoding cycle.

21. However, Ishikawa has taught that there are cycles performing operations before the execution cycle of instructions (Ishikawa column 2, lines 40-51 and column 4, lines 52-59). Grochowski has taught pipelining processor with

a. An instruction fetch pipeline (Grochowski column 7, lines 7-10 and Figure 1);

b. A storage circuit storing after an instruction fetch request is issued and before each fetch instruction is decoded in a decoding cycle of the instruction execution pipeline (Grochowski column 7, lines 7-10; 27-32; and 42-60 and Figure 1); and

c. A control circuit controlling after the fetched instruction is decoded hi the decoding cycle (Grochowski column 7, lines 7-10 and 34-41; column 8, lines 13-31; and Figure 1).

22. A person of ordinary skill in the art at the time the invention was made, and as supported by Grochowski, would have recognized that a pipeline divides the multiple cycles it takes to execute an instruction into steps or stages to overlap execution of instructions, which increases instruction processing speed (Grochowski column 1, lines 46-47 and column 2, lines 10-48). Therefore, it would have been obvious to a person of

ordinary skill in the art at the time the invention was made to incorporate the pipeline of Grochowski in the device of Ishikawa to increase processing speed.

23. In addition, Ishikawa has not taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system. Tran has taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system (Tran Abstract, lines 2-17; column 3, lines 22-51; column 5, lines 23-62; and column 8, lines 17-22). In regards to Tran, fetching instructions concurrently is out-of-order, meaning the instructions are not sequentially fetched. A person of ordinary skill in the art at the time the invention was made, and as supported by Tran, would have recognized that, by fetching and executing the instructions out of order, the pipeline is fully utilized (Tran column 3, lines 42-44), thereby increasing performance (Tran column 3, lines 44-45). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the out-of-order system of Tran in the device of Ishikawa to increase processor performance.

24. Referring to claim 12, Ishikawa has taught an instruction processing method using an instruction fetch pipeline and an instruction execution pipeline to perform an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

a. Handling mode information of an information processing apparatus, which is to be determined when fetching each instruction, as part of an instruction address (Ishikawa column 1, lines 13-17).

b. Fetching an instruction (Ishikawa column 3, lines 23-25).

c. Storing mode information of the fetched instruction as part of an instruction address of the fetched instruction in each cycle of an instruction process of the fetched instruction (Ishikawa column 1, lines 43-52).

d. Controlling the instruction process for the fetched instruction based on the stored mode information that has been stored (Ishikawa column 3, lines 25-35 and 43-64).

e. When the fetched instruction is a branch instruction and is not accompanied by a mode change, using the mode information that has been stored as mode information of a branch destination of the branch instruction (Ishikawa column 4, lines 20-27; Figure 2; and Figure 11).

25. Ishikawa has not explicitly taught a pipeline

a. Storing mode information after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the instruction execution pipeline.

b. Controlling the instruction process after the fetched instruction is decoded in the decoding cycle.

26. However, Ishikawa has taught that there are cycles performing operations before the execution cycle of instructions (Ishikawa column 2, lines 40-51 and column 4, lines 52-59). Grochowski has taught pipelining processor with

a. Storing mode information after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a

decoding cycle of the instruction execution pipeline (Grochowski column 7, lines 7-10; 27-32; and 42-60 and Figure 1).

b. Controlling the instruction process after the fetched instruction is decoded in the decoding cycle (Grochowski column 7, lines 7-10 and 30-34; column 7, line 61 to column 8, line 12; and Figure 1).

27. A person of ordinary skill in the art at the time the invention was made, and as supported by Grochowski, would have recognized that a pipeline divides the multiple cycles it takes to execute an instruction into steps or stages to overlap execution of instructions, which increases instruction processing speed (Grochowski column 1, lines 46-47 and column 2, lines 10-48). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipeline of Grochowski in the device of Ishikawa to increase processing speed.

28. In addition, Ishikawa has not taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system. Tran has taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system (Tran Abstract, lines 2-17; column 3, lines 22-51; column 5, lines 23-62; and column 8, lines 17-22). In regards to Tran, fetching instructions concurrently is out-of-order, meaning the instructions are not sequentially fetched. A person of ordinary skill in the art at the time the invention was made, and as supported by Tran, would have recognized that, by fetching and executing the instructions out of order, the pipeline is fully utilized (Tran column 3, lines 42-44), thereby increasing performance (Tran column 3, lines 44-45). Therefore, it would have been obvious to a person of ordinary skill in the

art at the time the invention was made to incorporate the out-of-order system of Tran in the device of Ishikawa to increase processor performance.

29. Referring to claim 13, Ishikawa has taught an instruction processing device provided with an instruction fetch pipeline and an instruction execution pipeline and performing an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

a. A storage means for storing a combination of address mode information of a fetched instruction and an instruction address of the fetched instruction (Ishikawa column 1, lines 43-52).

b. Branch instruction control means for controlling a branch instruction using the address mode information stored in the storage means if the fetched instruction is the branch instruction (Ishikawa column 2, lines 29-5).

c. Transfer means for transferring the address mode information stored in the storage means to the branch instruction control means when the branch instruction is executed (Ishikawa column 4, lines 20-27).

d. The branch instruction control means controlling the branch instruction using the address mode information transferred thereto as a branch destination of the branch instruction if the branch instruction is not accompanied by an address mode change (Ishikawa column 4, lines 20-27; Figure 2; and Figure 11).

30. Ishikawa has not explicitly taught a pipeline

a. Storage means for storing after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the instruction execution pipeline;

b. Branch instruction control means for controlling after the fetched instruction is decoded in the decoding cycle; and

c. Transfer means for transferring in an execution cycle of the instruction execution pipeline.

31. However, Ishikawa has taught that there are cycles performing operations before the execution cycle of instructions (Ishikawa column 2, lines 40-51 and column 4, lines 52-59). Grochowski has taught pipelining processor with

a. Storage means for storing after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the instruction execution pipeline (Grochowski column 7, lines 7-10; 27-32; and 42-60 and Figure 1);

b. Branch instruction control means for controlling after the fetched instruction is decoded in the decoding cycle (Grochowski column 7, lines 7-10 and 30-34; column 7, line 61 to column 8, line 12; and Figure 1); and

c. Transfer means for transferring in an execution cycle of the instruction execution pipeline (Grochowski column 7, lines 7-10 and 34-41; column 8, lines 13-31; and Figure 1).

32. A person of ordinary skill in the art at the time the invention was made, and as supported by Grochowski, would have recognized that a pipeline divides the multiple cycles it takes to execute an instruction into steps or stages to overlap execution of

instructions, which increases instruction processing speed (Grochowski column 1, lines 46-47 and column 2, lines 10-48). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipeline of Grochowski in the device of Ishikawa to increase processing speed.

33. In addition, Ishikawa has not taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system. Tran has taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system (Tran Abstract, lines 2-17; column 3, lines 22-51; column 5, lines 23-62; and column 8, lines 17-22). In regards to Tran, fetching instructions concurrently is out-of-order, meaning the instructions are not sequentially fetched. A person of ordinary skill in the art at the time the invention was made, and as supported by Tran, would have recognized that, by fetching and executing the instructions out of order, the pipeline is fully utilized (Tran column 3, lines 42-44), thereby increasing performance (Tran column 3, lines 44-45). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the out-of-order system of Tran in the device of Ishikawa to increase processor performance.

34. Referring to claim 14, Ishikawa has taught an instruction processing device provided with an instruction fetch pipeline and an instruction execution pipeline and performing an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

a. A storage means for storing a combination of mode information of a fetched instruction and an instruction address of the fetched instruction (Ishikawa column 1, lines 43-52).

b. Branch instruction control means for controlling a branch instruction using the mode information stored in the storage means if the fetched instruction is the branch instruction (Ishikawa column 2, lines 29-5).

c. Transfer means for transferring the mode information stored in the storage means to the branch instruction control means when the branch instruction is executed (Ishikawa column 4, lines 20-27).

d. The branch instruction control means controlling the branch instruction using the mode information transferred thereto, as a branch destination of the branch instruction if the branch instruction is not accompanied by an address mode change (Ishikawa column 4, lines 20-27; Figure 2; and Figure 11).

35. Ishikawa has not explicitly taught a pipeline

a. Storage means for storing after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the instruction execution pipeline;

b. Branch instruction control means for controlling after the fetched instruction is decoded in the decoding cycle; and

c. Transfer means for transferring in an execution cycle of the instruction execution pipeline.

36. However, Ishikawa has taught that there are cycles performing operations before the execution cycle of instructions (Ishikawa column 2, lines 40-51 and column 4, lines 52-59). Grochowski has taught pipelining processor with

a. Storage means for storing after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the instruction execution pipeline (Grochowski column 7, lines 7-10; 27-32; and 42-60 and Figure 1);

b. Branch instruction control means for controlling after the fetched instruction is decoded in the decoding cycle (Grochowski column 7, lines 7-10 and 30-34; column 7, line 61 to column 8, line 12; and Figure 1); and

c. Transfer means for transferring in an execution cycle of the instruction execution pipeline (Grochowski column 7, lines 7-10 and 34-41; column 8, lines 13-31; and Figure 1).

37. A person of ordinary skill in the art at the time the invention was made, and as supported by Grochowski, would have recognized that a pipeline divides the multiple cycles it takes to execute an instruction into steps or stages to overlap execution of instructions, which increases instruction processing speed (Grochowski column 1, lines 46-47 and column 2, lines 10-48). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipeline of Grochowski in the device of Ishikawa to increase processing speed.

38. In addition, Ishikawa has not taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system. Tran has taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system (Tran Abstract, lines 2-17; column 3, lines 22-51; column 5, lines 23-62; and column 8, lines 17-22). In regards to Tran, fetching instructions concurrently is out-of-order, meaning the instructions are not sequentially fetched. A person of ordinary

skill in the art at the time the invention was made, and as supported by Tran, would have recognized that, by fetching and executing the instructions out of order, the pipeline is fully utilized (Tran column 3, lines 42-44), thereby increasing performance (Tran column 3, lines 44-45). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the out-of-order system of Tran in the device of Ishikawa to increase processor performance.

39. Referring to claim 15, Ishikawa has taught an instruction processing device provided with an instruction fetch pipeline and an instruction execution pipeline and performing an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

a. Fetching means for fetching an instruction (Ishikawa column 3, lines 23-25).

b. Storage means for storing mode information of each fetched instruction as a part of an instruction address of the fetched instruction (Ishikawa column 1, lines 43-52).

c. Control means for controlling an instruction process of each instruction based on the stored mode information stored in the storage means (Ishikawa column 3, lines 25-35 and 43-64).

d. The control means controlling a branch instruction using the mode information stored in the storage means as mode information of a branch destination of the branch instruction if the fetched instruction is the branch instruction and is not accompanied by a mode change (Ishikawa column 4, lines 20-27; Figure 2; and Figure 11).

40. Ishikawa has not explicitly taught a pipeline

a. Storage means for storing after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the instruction execution pipeline; and

b. Control means for controlling after the fetched instruction is decoded in the decoding cycle.

41. However, Ishikawa has taught that there are cycles performing operations before the execution cycle of instructions (Ishikawa column 2, lines 40-51 and column 4, lines 52-59). Grochowski has taught pipelining processor with

a. Storage means for storing after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the instruction execution pipeline (Grochowski column 7, lines 7-10; 27-32; and 42-60 and Figure 1); and

b. Control means for controlling after the fetched instruction is decoded in the decoding cycle (Grochowski column 7, lines 7-10 and 30-34; column 7, line 61 to column 8, line 12; and Figure 1).

42. A person of ordinary skill in the art at the time the invention was made, and as supported by Grochowski, would have recognized that a pipeline divides the multiple cycles it takes to execute an instruction into steps or stages to overlap execution of instructions, which increases instruction processing speed (Grochowski column 1, lines 46-47 and column 2, lines 10-48). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipeline of Grochowski in the device of Ishikawa to increase processing speed.

43. In addition, Ishikawa has not taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system. Tran has taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system (Tran Abstract, lines 2-17; column 3, lines 22-51; column 5, lines 23-62; and column 8, lines 17-22). In regards to Tran, fetching instructions concurrently is out-of-order, meaning the instructions are not sequentially fetched. A person of ordinary skill in the art at the time the invention was made, and as supported by Tran, would have recognized that, by fetching and executing the instructions out of order, the pipeline is fully utilized (Tran column 3, lines 42-44), thereby increasing performance (Tran column 3, lines 44-45). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the out-of-order system of Tran in the device of Ishikawa to increase processor performance.

44. Referring to claim 17, Ishikawa has taught an instruction processing device provided with an instruction fetch pipeline and an instruction execution pipeline and performing an instruction fetch and an instruction execution by way of an out-of-order system, comprising:

a. A storage circuit to store a combination of mode information and an instruction address for the instructions to be fetched (Ishikawa column 1, lines 43-52).

b. A branch instruction control circuit to control execution of a branch instruction using the mode information stored in said storage circuit after one of the instructions to be fetched has been fetched as the branch instruction (Ishikawa column 2, lines 29-50).

c. A transfer circuit to transfer the mode information stored in said storage circuit to the branch instruction control circuit when the branch instruction is executed (Ishikawa column 4, lines 20-27 and Figure 1, element 11).

d. Said branch instruction control circuit controlling the branch instruction using the address mode information transferred thereto, as a branch destination of the branch instruction if the branch instruction is not accompanied by an address mode change (Ishikawa column 4, lines 20-27; Figure 2; and Figure 11).

45. Ishikawa has not explicitly taught a pipeline

a. A storage circuit to store after an instruction fetch request is issued in the instruction fetch pipeline and before a fetched instruction is decoded in a decoding cycle of the instruction execution pipeline;

b. A branch instruction control circuit decoded in the decoding cycle; and

c. A transfer circuit to transfer in an execution cycle of the instruction execution pipeline.

46. However, Ishikawa has taught that there are cycles performing operations before the execution cycle of instructions (Ishikawa column 2, lines 40-51 and column 4, lines 52-59). Grochowski has taught pipelining processor with

a. A storage circuit to store after an instruction fetch request is issued in the instruction fetch pipeline and before a fetched instruction is decoded in a decoding cycle of the instruction execution pipeline (Grochowski column 7, lines 7-10; 27-32; and 42-60 and Figure 1);

b. A branch instruction control circuit decoded in the decoding cycle (Grochowski column 7, lines 7-10 and 30-34; column 7, line 61 to column 8, line 12; and Figure 1); and

c. A transfer circuit to transfer in an execution cycle of the instruction execution pipeline (Grochowski column 7, lines 7-10 and 34-41; column 8, lines 13-31; and Figure 1).

47. A person of ordinary skill in the art at the time the invention was made, and as supported by Grochowski, would have recognized that a pipeline divides the multiple cycles it takes to execute an instruction into steps or stages to overlap execution of instructions, which increases instruction processing speed (Grochowski column 1, lines 46-47 and column 2, lines 10-48). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipeline of Grochowski in the device of Ishikawa to increase processing speed.

48. In addition, Ishikawa has not taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system. Tran has taught the instruction fetch pipeline and the instruction execution pipeline operate by way of the out-of-order system (Tran Abstract, lines 2-17; column 3, lines 22-51; column 5, lines 23-62; and column 8, lines 17-22). In regards to Tran, fetching instructions concurrently is out-of-order, meaning the instructions are not sequentially fetched. A person of ordinary skill in the art at the time the invention was made, and as supported by Tran, would have recognized that, by fetching and executing the instructions out of order, the pipeline is fully utilized (Tran column 3, lines 42-44), thereby increasing performance (Tran column 3, lines 44-45). Therefore, it would have been obvious to a person of ordinary skill in the

art at the time the invention was made to incorporate the out-of-order system of Tran in the device of Ishikawa to increase processor performance.

49. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa, U.S. Patent Number 5,142,630 (herein referred to as Ishikawa) in view of Grochowski et al., U.S. Patent Number 5,442,756 (herein referred to as Grochowski) and in further view of Tran, U.S. Patent Number 5,752,259 (herein referred to as Tran), as applied to claims 1 and 2 above, and in further view of Morisada, U.S. Patent Number 4,881,170 (herein referred to as Morisada).

50. Referring to claim 4, Ishikawa has not taught wherein said branch instruction control judges whether address mode information and an instruction address of a branch destination predicted by a branch prediction are correct using the address mode information and instruction address of the branch destination. Morisada has taught wherein said branch instruction control judges whether address mode information and an instruction address of a branch destination predicted by a branch prediction (Morisada Abstract, lines 12-16) are correct using the address mode information and instruction address of the branch destination (Morisada column 3, lines 45-52). A person of ordinary skill in the art at the time the invention was made would have recognized that this prevents an access to memory in the wrong mode during prefetching, which would decrease execution time. Therefore, it would have been obvious to a person of ordinary skill in the art to incorporate the prediction of Morisada in the device of Ishikawa to decrease execution time of instructions.

51. Referring to claim 7, Ishikawa has not taught the device further comprising a branch history circuit relating address mode information and an instruction address of a

branch instruction to address mode information and an instruction address of a branch destination, storing related address mode information and instruction addresses of the branch instruction and branch destination, and making a branch prediction for the fetched branch instruction. Morisada has taught a branch history circuit relating address mode information and an instruction address of a branch instruction to address mode information and an instruction address of a branch destination, storing related address mode information and instruction addresses of the branch instruction and branch destination, and making a branch prediction for the fetched branch instruction (Morisada Abstract, lines 4-16). A person of ordinary skill in the art at the time the invention was made would have recognized that to incorporate the branch history circuit of Morisada would allow branch prediction, which increases the speed of a processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the branch history circuit of Morisada in the device of Ishikawa to increase processor speed.

52. Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa, U.S. Patent Number 5,142,630 (herein referred to as Ishikawa) in view of in view of Tran, U.S. Patent Number 5,752,259 (herein referred to as Tran).

53. Referring to claims 11 and 16, Ishikawa has taught an instruction processing device comprising:

a. A plurality of storage circuits each storing a plurality of combinations of mode information of an instruction to be fetched and an instruction address of the instruction (Ishikawa column 1, lines 43-52 and column 3, lines 23-25);

b. A fetch circuit performing an instruction fetch based on mode information (Ishikawa column 4, lines 20-59).

c. Continuing an instruction fetch based on the mode information if a branch is performed according to the branch instruction (Ishikawa column 4, lines 20-27 and 39-59; Figure 2; and Figure 11).

54. Ishikawa has not taught

a. Instruction fetch ports which operate by way of the out-of-order system and

b. Performing an instruction pre-fetch of a branch destination of a branch instruction.

55. Tran has taught

a. Instruction fetch ports which operate by way of the out-of-order system (Tran Abstract, lines 2-17; column 3, lines 22-51; and column 5, lines 23-62) and

b. Performing an instruction pre-fetch of a branch destination of a branch instruction (Tran column 6, lines 37 to column 7, line 20 and Figure 1).

56. In regards to Tran, fetching instructions concurrently is out-of-order, meaning the instructions are not sequentially fetched. A person of ordinary skill in the art at the time the invention was made, and as supported by Tran, would have recognized that, by fetching and executing the instructions out of order the pipeline, is fully utilized (Tran column 3, lines 42-44), thereby increasing performance (Tran column 3, lines 44-45). Therefore, it would have been obvious to a person of ordinary skill in the art at the time

the invention was made to incorporate the out-of-order system of Tran in the device of Ishikawa to increase processor performance.

Response to Arguments

57. Applicant's arguments filed 22 February 2005 have been fully considered but they are not persuasive. Applicant's argue in essence

> "...the term 'address mode' refers to the size of the address space, i.e. whether the address is 24 bits or 31 bits. No suggestion has been cited or found in Tran of different address modes or sizes of the address space being taken into account by an out-of-order execution system...the combination of these three references lack any suggestion of how an out-of-order execution system could take different address modes, or address space sizes into account."

58. This has not been found persuasive. The most common definition for "address mode" in the art refers to how memory is accessed, i.e. register, absolute, indirect, etc., not the address size. Please see the accompanying definitions of "address mode" or "addressing mode". Because of this ambiguity in the definition, the limitation that "address mode" refers to the size of the address space must be incorporated into the claim language. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., addressing mode means the size of the address space) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

59. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

60. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

61. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
16 May 2005

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